Remarks

I. Status of claims

Claims 1-21 are pending.

Claims 1 and 15 are independent claims.

Claims 2-14 and 21 depend from independent claim 1 and claims 16-20 depend from independent claim 15.

II. Claim rejections

A. The rejection of claims 1-9 and 21 over Hideshima and Wu

The Examiner has rejected claims 1-9 and 21 under 35 U.S.C. § 103(a) over Hideshima (U.S. 5,143,865) in view of Wu (U.S. 2003/0067057).

1. Independent claim 1

Independent claim 1 recites:

> Claim 1 (original): An integrated circuit system, comprising:
>
> a die incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization and a top side thermal dissipation metallization, and the bottom side supporting a bottom side thermal dissipation metallization.

In the rejection of independent claim 1, the Examiner has stated that Hideshima "does not disclose a top side thermal dissipation metallization" (see page 2, ¶ 4, line 5, of the Office action). In an effort to make-up for this failure of Hideshima's disclosure, the Examiner has relied on the teachings of Wu. In particular, the Examiner has taken the position that (see pages 2-3, ¶ 4, lines 5-10, of the Office action):

> ... Nevertheless, Wu (e.g. fig. 3A) shows a die a topside thermal dissipation metallization 21. This type of embodiment

> allows the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package (pp 0009)....

In FIG. 3A, Wu shows a semiconductor package 2 that includes a semiconductor chip (or die) 23 that is bonded to a lead frame and is encapsulated by an encapsulant 25. The lead frame has leads 222 and a die pad 21, which are formed by a half-etching process (see ¶ 34, line 5 and lines 15-20). Solder bumps 24 bond contact pads on the active surface 230 of the semiconductor chip 23 to the leads 222, and a non-conductive thermal adhesive 212 bonds the active surface 230 of the semiconductor chip 23 to the die pad 21.

Contrary to the Examiner's statement, the die pad 21 does not constitute a top side thermal dissipation metallization that is supported on the top side of the semiconductor chip 23. First, the die pad 21 is not a "metallization" as defined in the specification. On page 4, lines 3-4, the specification recites that "As used herein, the term 'metallization' refers to single-layer metal film or a multi-layer metal film formed in or on an integrated circuit." The die pad 21 does not constitute a single-layer metal film or a multi-layer metal film. Instead, the die pad 21 is an integral component of a package lead frame that is adhesively bonded to the semiconductor chip 23 only when the semiconductor chip 23 is mounted in the package 2 (see FIG. 2B, which shows the die pad 110 as an integral component of the lead frame 10). Thus, one skilled in the art at the time the invention was made would not have considered the die pad 21 to be a "thermal dissipation metallization" as recited in claim 1. Second, there is no reasonable interpretation of the word "supported" that could read on the die pad 21, which operates to stop the semiconductor chip 23 from moving downwardly during the process of reflowing the solder bumps 24 (see, e.g., ¶ 34, lines 10-15; see also ¶ 31). Third, in Wu's disclosure, bonding pads are the only elements that are supported on the top side of the semiconductor chip 23 (see, e.g., FIG. 3A). One skilled in the art at the time the invention was made reasonably would infer from this disclosure, that the top surface of the semiconductor chip 23 is devoid of any type of structural elements designed to dissipate heat through the adhesive 212 and the die pad 21.

In summary, neither Hideshima nor Wu teaches anything about a die that has a top side supporting top side thermal dissipation metallization as recited in claim 1. Therefore, the combination of Hideshima and Wu cannot possibly teach or suggest the invention defined by

independent claim 1. For at least this reason, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) over Hideshima and Wu should be withdrawn.

The rejection of claim 1 under 35 U.S.C. § 103(a) over Hideshima in view of Wu also should be withdrawn because this rejection relies on an impermissible combination of the teachings of Hideshima and Wu.

The Examiner has stated that (see page 3, ¶ 4, lines 10-15, of the Office action):

> ... It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a top side thermal dissipation metallization layer as disclosed by Wu to allow the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package as suggested by Wu.

This rationale, however, does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 (see MPEP § 706.02(j)).

First, the Examiner's rationale is not based on a suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings (see the first prong of the test explained in MPEP § 706.02(j)). In particular, neither Hideshima nor Wu teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. In accordance with Hideshima's teaching only the bottom side of the semiconductor chip supports a thermal dissipation metallization (i.e., the solder layer 45C). Putting to one side the fact that Wu does not teach that the semiconductor chip 23 has any side that supports a thermal dissipation metallization, heat is dissipated out of the semiconductor chip 23 primarily through the active surface 230 of the semiconductor chip 23 via the non-conductive thermal adhesive 212 and the lead frame. Thus, neither Hideshima nor Wu teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. Therefore, one skilled in the art at the time the invention was made would not have had any motivation to modify Hideshima's teachings in the manner proposed by the Examiner.

Second, one skilled in the art at the time the invention was made would not have had a reasonable expectation that the Examiner's proposed modification of Hideshima's teachings would be successful (see the first prong of the test explained in MPEP § 706.02(j)). In

particular, the Examiner's position is that one skilled in the art would have been motivated to attach Wu's die pad 21 to the top side of Hideshima's semiconductor chip 10. As explained above, however, the die pad 21 and the leads 222 are integral components of the lead frame (see, e.g., FIG. 2B of Wu). Therefore, it is not possible to simply attach the die pad 21 to the central portion of the top side of Hideshima's semiconductor chip 10 without the other portions of the lead frame. As shown in FIG. 4 of Hideshima, however, such a modification would short circuit the emitter regions 13 and the collector electrode 16 in Hideshima's semiconductor chip (see, e.g., FIG. 8). The fact is that the semiconductor chips disclosed in Hideshima and Wu have different electrical connection needs. As a result, one skilled in the art would have to modify of the teachings of both references in ways that neither reference teaches or suggests in order to arrive at the inventive integrated circuit system defined in claim 1.

For the reasons explained above, it appears that the Examiner impermissibly has engaged in hindsight reconstruction of the claimed invention, using applicants' disclosure as a blueprint for piecing together the cited prior art to defeat patentability. Without a proper explanation for combining the cited prior art to arrive at the invention recited in claim 1, the Examiner has failed to establish a proper *prima facie* case of obviousness and the rejection of claim 1 should be withdrawn for this additional reason.

2. Dependent claims 2-9 and 21

Each of claims 2-9 and 21 incorporates the features of independent claim 1 and therefore is patentable over Hideshima and Wu for at least the same reasons explained above. Claims 8 and 9 also are patentable over Hideshima and Wu for the following additional reasons.

Claim 8 recites that the patterned metal layer comprises at least one through-hole. The Examiner has stated that "Hideshima shows that the patterned metal layer comprises at least one through-hole" (see page 3, ¶ 11 of the Office action). In the rejection of claim 1, however, the Examiner took the position that the die pad 21 shown in FIG. 3A constitutes a top side thermal dissipation that is supported by the top surface of the semiconductor chip 23. As shown clearly in FIG. 3A, the die pad 21 does not include at least one through-hole. For

at least this additional reason, the Examiner's rejection of claim 8 under 35 U.S.C. § 103(a) over Hideshima in view of Wu should be withdrawn.

Claim 9 depends from claim 8 and recites that the patterned metal layer comprises an array of through-holes. Claim 9 is patentable over Hideshima and Wu for the same additional reasons explained above in connection with claim 8.

B. The rejection of claims 1-4 and 6-11 over Hideshima and Kunikiyo

The Examiner has rejected claims 1-4 and 6-11 under 35 U.S.C. § 103(a) over Hideshima (U.S. 5,143,865) in view of Kunikiyo (U.S. 6,717,267).

1. Independent claim 1

In the rejection of independent claim 1, the Examiner has stated that Hideshima "does not disclose a top side thermal dissipation metallization" (see page 4, ¶ 15, lines 5-6, of the Office action). In an effort to make-up for this failure of Hideshima's disclosure, the Examiner has relied on the teachings of Kunikiyo. In particular, the Examiner has taken the position that (see pages 2-3, ¶ 4, lines 5-10, of the Office action):

> ... Nevertheless, Kunikiyo (e.g. fig. 19) shows a top side thermal dissipation metallization 31. According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lis. 1-18)....

In FIG. 19, Kunikiyo discloses a semiconductor device that includes dummy interconnections 9a-b, 21a-c, and 25a-c, dummy plugs 22a-b, 26a-c, 29b-c, and 31, and a heat sink 32. The dummy interconnections are formed in order to improve the flatness in the CMP processes used in the formation of the semiconductor device and to correct the proximity effect in which the finished resist form is affected by the proximate pattern form in the transfer processes used in the formation of the semiconductor device (see, e.g., col. 5, lines 46-50). The dummy plugs 22a-b, 26a-c, and 29b-c serve to connect the dummy

interconnections to ground potential in order to reduce noise (see, e.g., col. 10, lines 28-38). The dummy plugs 31 serve to transfer heat from the interlayer insulating films to the heat sink 32, which dissipates the heat.

Contrary to the Examiner's statement, the dummy plugs 31 do not constitute a "thermal dissipation metallization."

First, the dummy plugs 31 do not constitute a "metallization" as defined in the specification. On page 4, lines 3-4, the specification of the instant application recites that "As used herein, the term "metallization" refers to single-layer metal film or a multi-layer metal film formed in or on an integrated circuit." The dummy plugs 31 do not constitute a single-layer metal film or a multi-layer metal film. Instead, the dummy plugs 31 constitute a small number of spaced apart metal plugs that are positioned only where the dummy interconnections are located and are formed by filling through holes in the passivation film 30 with metal and chemically-mechanically removing excess metal until the top surfaces of the plugs 31 and the passivation film 30 coincide (see, e.g., FIG. 19 and col. 11, line 36 - col. 12, line 23).

Second, the dummy plugs 31 do not constitute a "thermal dissipation" metallization in accordance with the ordinary and accustomed meaning of the term "thermal dissipation." In accordance with its ordinary and accustomed meaning, the word "dissipation" refers to the action or process of breaking up and driving off or causing to spread thin or scatter and gradually vanish (see, e.g., Merriam-Webster's Collegiate Dictionary, 10th Ed.). The word "thermal" means "of, relating to, or caused by heat" (see, e.g., Merriam-Webster's Collegiate Dictionary, 10th Ed.). The dummy plugs 31 do not break up and drive off heat nor do they cause heat to spread thin or scatter and gradually vanish. Instead, the dummy plugs 31 merely conductor heat from the regions of the interlayer insulating films near the dummy interconnections to the heat sink 32, which dissipates the heat.

Thus, one skilled in the art at the time the invention was made reasonably would not have considered the dummy plugs 31 to be a "thermal dissipation metallization" as recited in claim 1. Since neither Hideshima nor Kunikiyo teaches or suggests anything about a die that has a top side supporting top side thermal dissipation metallization as recited in claim 1, the combination of Hideshima and Kunikiyo cannot possibly teach or suggest the invention defined by independent claim 1. For at least this reason, the Examiner's rejection of

independent claim 1 under 35 U.S.C. § 103(a) over Hideshima and Kunikiyo should be withdrawn.

The rejection of claim 1 under 35 U.S.C. § 103(a) over Hideshima in view of Kunikiyo also should be withdrawn because this rejection relies on an impermissible combination of the teachings of Hideshima and Kunikiyo.

The Examiner has stated that (see pages 4-5, ¶ 15, lines 12-16, of the Office action):

> ... It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in Hideshima's invention a topside thermal dissipation metallization such as dummy patterns in accordance to Kunikiyo's invention to improve the circuit operation since the heat can be satisfactorily removed form the interlayer insulating films.

This rationale, however, does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 (see MPEP § 706.02(j)).

First, the Examiner's rationale is not based on a suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings (see the first prong of the test explained in MPEP § 706.02(j)).

Neither Hideshima nor Kunikiyo teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. In accordance with Hideshima's teaching only the bottom side of the semiconductor chip supports a thermal dissipation metallization (i.e., the solder layer 45C). Putting to one side the fact that Kunikiyo does not teach that the semiconductor device shown in FIG. 19 has any side that supports a thermal dissipation metallization, heat is dissipated out of the semiconductor device only through the top side of the semiconductor device via the heat sink 32. Thus, neither Hideshima nor Kunikiyo teaches or suggests anything about supporting thermal dissipation metallizations on both top and bottom sides of a die. Therefore, one skilled in the art at the time the invention was made would not have had any motivation to modify Hideshima's teachings in the manner proposed by the Examiner.

Furthermore, neither Hideshima nor Kunikiyo teaches or suggest anything that would have led one skilled in the art at the time the invention was made to incorporate Kunikiyo's dummy plugs 31 in the insulating film 17 of Hideshima's semiconductor device 10, as proposed by the Examiner. Hideshima does not teach or suggest anything about dummy

plugs and dummy interconnections. In accordance with Kunikiyo's teachings, the dummy plugs 31 only serve to connect the underlying dummy interconnections to the heat sink 32. Since there are no dummy interconnection in Hideshima's semiconductor device 10, one skilled in the art would not have had any motivation to incorporate the dummy plugs 10 in Hideshima's semiconductor device.

Second, one skilled in the art at the time the invention was made would not have had a reasonable expectation that the Examiner's proposed modification of Hideshima's teachings would be successful (see the first prong of the test explained in MPEP § 706.02(j)). In particular, the Examiner's position is that one skilled in the art would have been motivated to incorporate Kunikiyo's plugs 31 in the insulating film 17 on the top side of Hideshima's semiconductor chip 10. As explained above, however, the dummy plugs 31 only serve to connect the underlying dummy interconnections to the heat sink 32, which covers the entire top surface of Kunikiyo's semiconductor device (see FIG. 19). It is not possible to attach a heat sink of the type disclosed in Kunikiyo on the top side of Hideshima's semiconductor chip 10 because, as shown in FIG. 4 of Hideshima, such a modification would interfere with the interconnection between the lead frame and the solder bumps on the top surface of Hideshima's semiconductor chip 10 (see, e.g., FIG. 8). The fact is that the semiconductor chips disclosed in Hideshima and Kunikiyo have different electrical connection needs. As a result, one skilled in the art would have had to modify of the teachings of both references in a way that neither reference teaches or suggests in order to arrive at the inventive integrated circuit system defined in claim 1.

For the reasons explained above, it appears that the Examiner impermissibly has engaged in hindsight reconstruction of the claimed invention, using applicants' disclosure as a blueprint for piecing together the cited prior art to defeat patentability. Without a proper explanation for combining the cited prior art to arrive at the invention recited in claim 1, the Examiner has failed to establish a proper *prima facie* case of obviousness and the rejection of claim 1 should be withdrawn for this additional reason.

2. Dependent claims 2-4 and 6-11

Each of claims 2-4 and 6-11 incorporates the features of independent claim 1 and therefore is patentable over Hideshima and Kunikiyo for at least the same reasons explained

above. Claims 8-11 also are patentable over Hideshima and Kunikiyo for the following additional reasons.

Claim 8 recites that the patterned metal layer comprises at least one through-hole. The Examiner has stated that "Hideshima shows that the patterned metal layer comprises at least one through-hole" (see page 3, ¶ 11 of the Office action). In the rejection of claim 1, however, the Examiner took the position that the die pad 21 shown in FIG. 3A constitutes a top side thermal dissipation that is supported by the top surface of the semiconductor chip 23. As shown clearly in FIG. 3A, the die pad 21 does not include at least one through-hole. For at least this additional reason, the Examiner's rejection of claim 8 under 35 U.S.C. § 103(a) over Hideshima in view of Kunikiyo should be withdrawn.

Claim 9 depends from claim 8 and recites that the patterned metal layer comprises an array of through-holes. Claim 9 is patentable over Hideshima and Kunikiyo for the same additional reasons explained above in connection with claim 8.

Claim 10 depends from claim 1 and additionally recites that the integrated circuit system includes a package comprising a top heat spreader metallurgically bonded to the top side thermal dissipation metallization of the die. In his rejection of claim 10, the Examiner has stated that Kunikiyo "shows a top heat spreader 32 metallurgically bonded (31) to the top side thermal dissipation metallization of the die (dummy pattern 25a)" (see ¶ 18 on page 5 of the final Office action). Kunikiyo discloses attaching a heat sink 32 to plugs 31 that are formed in a passivation film 30 (see col. 23, lines 1-18). Kunikiyo, however, does not teach or suggest how the heat sink 32 is attached to the plugs 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plugs 31, as recited in claim 10. For at least these reasons the Examiner's rejection of claim 10 under 35 U.S.C. § 103(a) over Hideshima and Kunikiyo should be withdrawn.

Claim 11 depends from claim 10 and therefore is patentable over Hideshima and Kunikiyo for at least the same reasons.

C. Claims 12 and 13

The Examiner has rejected claims 12 and 13 under 35 U.S.C. § 103(a) over Hideshima, Kunikiyo, and Wang (U.S. 5,977,626).

Each of claims 12 and 13 incorporates the features of claim 10. Wang does not make-up for the failure of Hideshima and Kunikiyo to teach or suggest the features discussed above in connection with claim 10. Indeed, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy (see col. 3, lines 49-53).

For at least these reasons the Examiner's rejection of claims 12 and 13 under 35 U.S.C. § 103(a) over Hideshima, Kunikiyo, and Wang should be withdrawn.

It is noted that Wang does not teach or suggest anything about either a top side thermal dissipation metallization or a back side thermal dissipation metallization.

D. Claim 14

The Examiner has rejected claim 14 under 35 U.S.C. § 103(a) over Hideshima, Kunikiyo, and Khan (U.S. 6,853,070).

Claim 14 incorporates the features of independent claim 10. Khan does not make-up for the failure of Hideshima and Kunikiyo to teach or suggest the features discussed above in connection with claim 10. Indeed, Khan clearly teaches that the drop-in heat spreader 202 is attached to the top side of the die 102 using an epoxy 204 (see FIG. 2A and col. 7, lines 29-31). In addition, Khan fails to teach or suggest anything about a top side thermal dissipation metallization.

For at least these reasons the Examiner's rejection of claim 14 under 35 U.S.C. § 103(a) over Hideshima in view of Kunikiyo and Khan should be withdrawn. The Examiner's rejection of claim 14 also should be withdrawn for the following additional reasons.

Claim 14 recites that the package further comprises a bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die. The Examiner has stated that "Khan (e.g., fig. 2A) shows a bottom heat spreader 110 bonded to the bottom side thermal dissipation metallization of the die 102." Khan, however, teaches that the heat spreader 110 is attached to the bottom side of the die 102 using an epoxy (see col. 4, lines 60-61). In addition, contrary to the Examiner's assumption, Khan does not teach or suggest that the die 102 includes a bottom side thermal dissipation metallization.

E. Claims 15-18

The Examiner has rejected claims 15-18 under 35 U.S.C. § 103(a) over Hideshima in view of White (U.S. 5,665,655) and Kunikiyo.

1. Independent claim 15

Independent claim 15 recites:

> Claim 15 (previously presented): A method of making an integrated circuit system, comprising:
>
> forming on a top side of a substrate multiple die regions each having a top side supporting an exposed electrical signal communication metallization and an exposed top side thermal dissipation metallization;
>
> forming on a bottom side of the substrate an exposed bottom side thermal dissipation metallization for each die region; and
>
> singulating the die regions to form respective integrated circuit dice.

Independent claim 15 recites features that essentially track the pertinent features discussed above in connection with independent claim 1. White does not make-up for the failure of Hideshima and Kunikiyo to teach or suggest the pertinent features of independent claim 1 discussed above. Indeed, the Examiner merely has cited White for showing "a method including the steps of forming multiple die regions on a substrate and the step of ... singulating the die regions to form the integrated circuit ... [dice]." Therefore, claim 15 is patentable over Hideshima in view of White and Kunikiyo for at least the same reasons explained above in connection with independent claim 1.

2. Dependent claims 16-18

Each of claims 16-18 incorporates the features of independent claim 15 and therefore is patentable over Hideshima, White, and Kunikiyo for at least the same reasons explained above.

Claim 18 also is patentable over Hideshima, White, and Kunikiyo for the following additional reasons.

In his rejection of claim 18, the Examiner has stated that Kunikiyo "shows the step of metallurgically bonding a top heat spreader of the package (e.g., 31) to the top side thermal dissipation metallization of the singulated die (dummy pattern 25a)." Kunikiyo, however, does not teach or suggest how the heat sink 32 is attached to the plug 31. Therefore, there is no support for the Examiner's assertion that the heat sink 32 is metallurgically bonded to the plug 31.

For at least these reasons the Examiner's rejection of claim 18 under 35 U.S.C. § 103(a) over Hideshima, White, and Kunikiyo should be withdrawn.

F. Claims 19 and 20

The Examiner has rejected claims 19 and 20 under 35 U.S.C. § 103(a) over Hideshima in view of White, Kunikiyo, and Wang.

Each of claims 19 and 20 incorporates the features of claim 18. Wang does not make-up for the failure of Hideshima, White, and Kunikiyo to teach or suggest the features discussed above in connection with independent claim 1. Indeed, Wang teaches that the heat spreader 32 is attached to the top side of the die 22 using an adhesive, such as a heat spreader attach epoxy (see col. 3, lines 49-53).

For at least these reasons the Examiner's rejection of claims 19 and 20 under 35 U.S.C. § 103(a) over Hideshima in view of White, Kunikiyo, and Wang should be withdrawn.

As noted above, Wang does not teach or suggest anything about either a top side thermal dissipation metallization or a back side thermal dissipation metallization.

III. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-3718.

Respectfully submitted,

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